REMARKS

Claims 17-37 will be pending upon entry of the present amendment. Claims 17, 24, and 30 are being amended. Claim 37 is being newly presented.

Claims 17-36 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Independent claims 17 and 24 are being amended as suggested by the Examiner. Independent claim 30 does not include the same informalities as claims 17 and 24, and thus, claim 30 is not being amended. Accordingly, claims 17-36 particularly point out and distinctly claim the invention.

Claims 24-26 were also rejected under 35 U.S.C. § 112, second paragraph, as being indefinite because the Examiner indicated that the meaning of "first and second capacitors being positioned in a first plane that is *transverse* to a second plane in which the second and third capacitors are position" is unclear.

The applicants respectfully submit that the language of claims 24-36 is clear and is supported by the specification. Figure 5 shows three capacitors that are lined up along a first plane (the face of the paper on which Figure 5 is drawn). Figure 6 is a cross-section taken along line VI-VI of Figure 5 and shows three capacitors lined up along a second plane (the face of the paper on which Figure 6 is drawn) that is transverse to the first plane. The middle capacitor of Figure 5 is one of the capacitors of Figure 6, and thus, is in both of the first and second planes.

In addition, Figure 9 shows a layout of two pairs of memory cells in which a continuous conductive layer 152 forms the upper plates of the capacitors of the memory cells and the conductive areas 50 are the lower plates (see also the cross-section of Figure 8). The capacitors along either row of Figure 9 are lined up in a first plane that is transverse to a second plane through either of the columns of capacitors of Figure 9. For example, the upper-left capacitor of Figure 9 is in a first plane that also includes the upper-right capacitor and the upper-left capacitor is also in a second plane that includes the lower-left capacitor.

For the foregoing reasons, claims 24-26 particularly point out and distinctly claim the invention.

Claims 17-36 were rejected under the judicially created doctrine of obviousness-type double patenting. Enclosed is a terminal disclaimer signed by an attorney of record.

Claims 17-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,350,705 to Brassington et al. ("Brassington").

Brassington does not disclose the invention recited in claims 17-23, as amended. In particular, claim 17 is directed to a memory array including a plurality of stacked cells in which each cell includes a MOS transistor; a capacitor formed directly above a first conduction region of the MOS transistor; and an electrical connector that contacts a bottom of a first plate of the capacitor. Brassington does not disclose any stacked memory cells, and instead, shows only strapped memory cells. As is well known in the art, such strapped cells occupy a much greater surface area of the semiconductor chip than stacked cells thereby preventing the strapped memory cells from being miniaturized as mandated by current memory standards.

Although the recitation of "stacked" memory cells in claim 17 is sufficient to distinguish the claimed invention from Brassington, the amendments to claim 17 further distinguish the invention from Brassington. In particular, Brassington does not disclose a capacitor that is formed directly above a first conduction region of the MOS transistor or an electrical connector that contacts a bottom of a first plate of the capacitor. Instead, Figure 3 of Brassington shows capacitors 12, 22 that are not directly above the drain regions 32, 34. Further, Figure 3 shows metal interconnects 54, 56 that are connected respectively to contact areas 68, 69 on the top sides of the plates 40, 42. In contrast to the connectors of stacked cells that contact the bottom surface of the bottom plates, such metal interconnects 54, 56 provide a less-reliable connection and occupy more surface area of the underlying semiconductor substrate.

For the foregoing reasons, claims 17-23 are not anticipated by Brassington.

Claims 24-26, 28-32, and 34-36 were rejected under 35 U.S.C. § 102 as being anticipated by Okudaira et al. ("Okudaira").

Okudaira does not disclose the invention recited in claims 24-26, 28-32, and 34-36. In particular, claim 24 recites a memory array having first and second stacked cells positioned in a first plane and a third stacked cell positioned with the second stacked cell in a second plane that is transverse to the first plane, wherein the respective capacitors of the cells have respective second plates that are continuous with one another. In contrast to the arrangement shown in Figure 9 of the present application in which the top plate 152 is shared by

capacitors in horizontal and vertical planes, the capacitors in Figure 1 of Okudaira are all positioned in the same plane. Every one of Okudaira's 82 figures, except for the circuit diagrams of Figures 71-72, is a cross-sectional view taken along the same plane, and thus, no second plane transverse to the first plane is even shown. As such, nothing in the figures or text of Okudaira suggests stacked cells with capacitors in transverse planes having respective second plates that are continuous with one another.

For the foregoing reasons, claims 24-26 and 28-29 are not anticipated by Okudaira.

Although the language of claims 30-32 and 34-36 is not identical to that of claim 24, the allowability of claims 30-32 and 34-36 will be apparent in view of the above discussion of claim 24.

Claims 27 and 33 were rejected under 35 U.S.C. § 103 as being unpatentable over Okudaira in view of Brassington.

Okudaira and Brassington do not teach or suggest the invention recited in claims 27 and 33, which depend on claims 24 and 30, respectively. Brassington does not teach or suggest all of the features of claims 24 and 30 that are missing from Okudaira. In particular, Brassington does not teach or suggest capacitors in transverse first and second planes having respective dielectric regions that are continuous with one another. As seen in Figures 2 and 3 of Brassington, the dielectric region 44 is shared by only two capacitors 12, 22 that are positioned in the same plane. The dielectric region 44 does not extend to any capacitor that would be adjacent to either of the capacitors 12, 22 in the vertical dimension of Figure 2. Accordingly, claims 27 and 33 are nonobvious in view of Okudaira and Brassington.

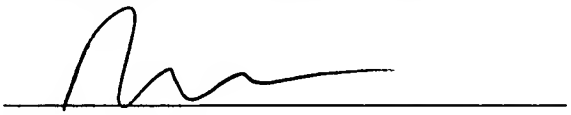
New claim 37 depends on claim 17 and further recites that the MOS transistors of the pair of cells are positioned in separate active regions that are separated from each other by an insulating region. Brassington does not disclose such an arrangement. Instead, Brassington shows that the transistors 14, 24 are formed in the same active region that is defined on opposite sides by field oxide regions 80. Accordingly, claim 37 is not anticipated by Brassington.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



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